

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

LISTING OF CLAIMS:

1. (Canceled)

2. (Currently Amended) A semiconductor device according to claim 1, formed on a single semiconductor chip, comprising:
a digital-signal-processing circuit;
a CPU controlling said digital-signal-processing circuit; and
an interface circuit inputting a digital signal synchronously with a first clock signal and supplying said input digital signal to said digital-signal-processing circuit and outputting digital data processed by said digital-signal-processing circuit synchronously with said first clock signal,
wherein said interface circuit includes:
an input circuit inputting a digital signal synchronously with said first clock signal and supplying said input digital signal to said digital-signal-processing circuit;
a gain-adjusting circuit adjusting a gain of said digital signal supplied to said input circuit; and
an output circuit adding said digital signal with said gain thereof adjusted to a digital signal supplied from said digital-signal-processing circuit and outputting a resulting digital signal synchronously with said first clock signal;
wherein said input circuit comprises:
an input shift register inputting and shifting ~~a-the~~ digital signal synchronously with said first clock signal; and
an input register latching ~~a-the~~ digital signal input and shifted in said input shift register synchronously with a second clock signal.

3. (Currently Amended) A semiconductor device according to claim 2, wherein said gain-adjusting circuit comprises:

a shifter ~~capable of~~ for inputting and shifting ~~a~~ the digital signal inputted and shifted by said input shift register; and

a gain control register controlling the number of shift operations carried out by said shifter.

4. (Currently Amended) A semiconductor device according to claim 3, wherein said output circuit comprises:

an output register latching ~~the digital signal~~ data processed by said digital-signal processing unit synchronously with said second clock signal;

an adder adding a signal output by said shifter to said latched digital data in said output register; and

an output shift register inputting a signal output by said adder and shifting and outputting said signal synchronously with said first clock signal.

5. (Currently Amended) A semiconductor device according to claim 3, wherein said CPU is ~~configured to access~~ capable of making an access to said gain control register to write data into said gain control register.

6. (Currently Amended) A semiconductor device according to claim 4, wherein said CPU is ~~configured to access~~ capable of making an access to said input register and said output register to write data into said input and output registers.

7. (Currently Amended) A semiconductor device according to claim 4, wherein:

an output stage of said input register and an output stage of said output register are each provided with a changeover switch selecting either said output stage or a value of 0;

select control information for driving said changeover switches is stored in a switch control register; and

said CPU is configured to access capable of making an access to said switch control register to write data into said switch control register.

8. (Currently Amended) A semiconductor device according to claim 1-2, wherein, in response to an interrupt signal, said CPU issues a command to said digital-signal-processing circuit, requesting said digital-signal-processing circuit to carry out processing operations.